EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	762	(712/23).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:22
S2	486	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:22
S3	0	(superscalar$1) same (issu$3 with way$1 with group$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:23
S4	7	(issu$3 with way$1 with (instruction$1 near4 group$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:26
S5	0	(issu$3 with (instruction$1 near4 group$3)) same (mutiple$1 near4 (process$3 or function$3) near4 (unit$1 or device$1 or element$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:27
S6	0	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) same (mutiple$1 near4 (process$3 or function$3) near4 (unit$1 or device$1 or element$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:27
S7	0	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) same (mutiple$1 near4 (process$3 or function$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S8	0	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) same (mutiple$1 with (process$3 or function$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S9	1	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) and (mutiple$1 with (process$3 or function$3))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:28
S10	132	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) and (integer near4 (float$3?point$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:29
S11	16	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) same (integer near4 (float$3?point$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39

S12	8	(("6038656") or ("5752070") or ("6044061") or ("5832303") or ("6230228") or ("5802055") or ("6279065") or ("6301630")).PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2006/04/05 13:32
S13	775	(712/23).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:33
S14	516	(712/215).CCLS.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:34
S15	728	(712/23).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/03/25 10:34
S16	520	(712/215).CCLS.	US-PGPUB; USPAT	OR	OFF	2007/03/25 10:34
S17	1	("20040111589").PN.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:36
S18	0	(asynchronous$5) near4 (issu$3 near4 instruction$1 near4 simulataneous$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:38
S19	0	(asynchronous$5) with (issu$3 near4 instruction$1 near4 simulataneous$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39
S20	0	(asynchronous$5) with (issu$3 with instruction$1 with simulataneous$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39
S21	0	(asynchronous$5) same (issu$3 with instruction$1 with simulataneous$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:39
S22	0	(asynchronous$5 near4 pipelin$3) and (issu$3 with instruction$1 with simulataneous$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 11:57
S23	37	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) same (integer near4 (float$3?point$1))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:40

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S24	14	(issu$3 with instruction$1 with (simultaneous$2 or concurrent$2)) same (integer near4 (float$3?point$1)) and ((asynchronous or independent) near4 pipelin$3)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:40
S25	2	((lines-andrew$) and (southworth-robert$) and (cummings-uri$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:44
S26	63	((lines-andrew$) or (southworth-robert$) or (cummings-uri$)).in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 10:44
S27	5	(asynchronous$5 near4 pipelin$3) same (sequential$4 near4 control$5)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2007/03/25 11:57

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S Furber
J Burch
N Paver
E Clarke
K McMillan

<u>Sequential circuit verification using symbolic model checking</u> - <u>group of 7 »</u>
JR Burch, EM Clarke, KL McMillan, DL Dill - Design Automation Conference, 1990. Proceedings. 27th ACM/ ..., 1990 -
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... algorithm on both synchronous and **asynchronous** (self-timed ... and Fisher [2] verifies
a **pipeline** circuit with ... Constraints Next, we consider the **issue** of fairness. ...
<u>Cited by 298</u> - <u>Related Articles</u> - <u>Web Search</u>

[BOOK] <u>Principles of Asynchoronous Circuit Design: A Systems Perspective</u> - <u>group of 7 »</u>
JEDT Spars, J Sparso. SB Furber, SB Furber - 2001 - books.google.com
... 6.1 Introduction 81 6.1.1 **Asynchronous sequential** circuits 81 6.1.2 Hazards ... 173 10.2
Data typing **issues** 176 ... 279 15.4.2 **Asynchronous pipeline** architectures 281 ...
<u>Cited by 117</u> - <u>Related Articles</u> - <u>Web Search</u> - <u>Library Search</u>

<u>Interfacing synchronous and **asynchronous** modules within ahigh-speed pipeline</u> - <u>group of 15 »</u>
AE Sjogren, CJ Myers - Very Large Scale Integration (VLSI) Systems, IEEE ..., 2000 - ieeexplore.ieee.org
... To solve this problem, we have added an additional **pipeline** reg- ister
after each **asynchronous** module. As depicted in Fig. ...
<u>Cited by 52</u> - <u>Related Articles</u> - <u>Web Search</u> - <u>BL Direct</u>

<u>Hades-Towards the Design of an **Asynchronous** Superscalar Processor</u> - <u>group of 4 »</u>
CJ Elston, DB Christianson, PA Findlay, GB Steven - ... Proceedings of the 2nd Working Conference on **Asynchronous** ... -
doi.ieeecomputersociety.org
... for instructions in proportion to the **issue** rate. ... method for resolving branches in
an **asynchronous** processor. ... delay region to provide the **pipeline** with useful ...
<u>Cited by 13</u> - <u>Related Articles</u> - <u>Web Search</u>

<u>Modeling and design of **asynchronous** circuits</u> - <u>group of 5 »</u>
MB Josephs, SM Nowick, CH Van Berkel - Proceedings of the IEEE, 1999 - ieeexplore.ieee.org
... However, for correct **sequential** operation, burst-mode requires ... In this Special **Issue**,
one paper [13 ... of the performance of **asynchronous pipelines**, and another ...
<u>Cited by 17</u> - <u>Related Articles</u> - <u>Web Search</u> - <u>BL Direct</u>

<u>**Asynchronous** design for programmable digital signal processors</u> - <u>group of 5 »</u>
THY Meng, RW Brodersen, DG Messerschmitt - Signal Processing, IEEE Transactions on [see also Acoustics, ..., 1991 -
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... level, where clock distribution is not an **Issue**. Interboard communications have
long used **asynchronous** ltnks (for ... processing delay among all **pipeline** stages. ...
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<u>AMULET2e: An **Asynchronous** Embedded Controller</u> - <u>group of 19 »</u>
SB FURBER, JD GARSIDE, P RIOCREUX, S TEMPLE, P DAY ... - PROCEEDINGS OF THE IEEE, 1999 - ieeexplore.ieee.org
... a lookup on every instruction address **Issue** it is ... nism stalls a **control** loop in the
execution **pipeline**. ... and RAM are self-timed for **asynchronous** operation using ...
<u>Cited by 120</u> - <u>Related Articles</u> - <u>Web Search</u> - <u>BL Direct</u>

<u>DDMPs: self-timed super-pipelined data-driven multimedia processors</u> - <u>group of 4 »</u>
H Terada, S Miyata, M Iwata - Proceedings of the IEEE, 1999 - ieeexplore.ieee.org
... been several attempts to introduce **asynchronous pipelines** into conventional ... 1981,
the clock skew problem was not ... used to interconnect the self-timed **pipelines**. ...
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<u>AMULET1: A Micropipelined ARM</u> - <u>group of 6 »</u>
SB Furber, P Day, JD Garside, NC Paver, JV Woods - ieeexplore.ieee.org
... some cases them are functionality **Issues** to consider ... longer than the PC **pipeline**
otherwise a ... 4: **Asynchronous** operation The **asynchronous** implementation of the ...
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<u>Special **Issue** On **Asynchronous** Circuits And Systems</u>
SM Nowick, MB Josephs, CH van Berkel - Proceedings of the IEEE, 1999 - ieeexplore.ieee.org
... 10 improvement over conventional **sequential** digital signal ... Properties of Linear
Asynchronous Pipelines," tackles a different problem: analytical techniques ...
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